operation clock rates, said sets of system operation signals stored in said memory so that said sets of system operation signals are retrievable.

10. (Amended three times) An integrated circuit comprising

an interface for coupling to an external diagnostic processor;

a unit responsive to instructions from said external diagnostic processor for capturing sets of sequential system operation signals of said integrated circuit;

a plurality of probe lines coupled to said unit for carrying said system operation signals from predetermined probe points of said integrated circuit, wherein said probe lines comprise strings of storage elements providing signal paths from said probe points to said unit, said signal paths capable of moving said sets of sequential system operation signals at system operation clock rates;

a memory coupled to said unit and to said interface, said sets of sequential system operation signals stored in said memory at one or more clock signal rates internal to said integrated circuit and retrieved from said memory through said interface to said external process at one or more clock signal rates external to said integrated circuit so that said external diagnostics processor can process said captured system operation signals.

15. (Amended three times) A method of operating an integrated circuit having logic blocks, a control unit, a memory and a plurality of probe lines of said logic blocks, said method comprising

operating said logic blocks to perform normal system operations at one or more system clock signal rates internal to said integrated circuit to produce sets of system operation signals;

enabling said probe lines responsive to said control unit to capture and carry said sets of system operation signals of said logic blocks at said system clock signal rates internal to said integrated circuit;

retrieving said sets of system operation signals from said logic blocks along said probe lines at said system clock signal rates internal to said integrated circuit,

storing said sets of system operation signals in said memory at said system clock signal rates internal to said integrated circuit; and

processing said sets of stored system operation signals to perform test and debug operations of said logic blocks of said integrated circuit.

REMARKS

Reconsideration of the present patent application, as supplementarily amended, is respectfully requested.

First, the undersigned attorney wishes to thank the Examiner for his courtesy and effort to expedite prosecution of the present application at the telephone interviews of July 23 and 26, 2001. At the first interview the Examiner informed the attorney of newly found U.S. Patent No. 5,495,486, which issued February 27, 1996 to T. Gheewala. In the subsequent interview on July 26, 2001, the undersigned attorney and Examiner discussed the relevance of the Gheewala reference with respect to applicants' pending independent claims 1 and 10. No agreement was reached, but the Examiner suggested that the applicants submit their arguments and any accompanying amendments in writing for full consideration. This supplemental amendment is a response to that suggestion.

From the interviews the applicants understand that the Examiner believes that the Gheewala '486 patent might teach the claimed "storage elements," added by the applicants in their Amendment of July 5, 2001. The applicants do not believe that the Gheewala patent has such a teaching for at least three reasons: 1) Unlike the applicants' claims, the "storage elements" of Gheewala are the integrated circuit constituents being tested and not constituents doing the testing; 2) Though having the same terminology as the applicants' claims, the "probe lines" of the Gheewala patent are control lines and do not carry system operation signals as called for by the applicants' claims; and 3) Even assuming that the sense lines of the Gheewala patent are to be analogized to the applicant's probe lines, the sense lines do not meet the language of the applicants' claims. Furthermore, to better point out their invention, the applicants have amended independent claims 1, 10 and 15 in this Supplemental Amendment.

In the first place, the Examiner has apparently assumed that from the similarity of language, i.e., "storage elements," that the Gheewala patent teaches the use of storage elements for observing the operations of an integrated circuit, as called for in the applicants' claims. The applicants' storage elements are recited as part of the probe lines in claims 1 and 10. In contrast, in the Gheewala patent, the "storage elements" are the constituents of the integrated circuit